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Application No.: 10/698,805 Docket No.: MWS-058

## REMARKS

In this Response, claims 1-5, 7-8, 32-35 and 42 have been amended. Claims 11-31, 38-41 and 43-44 were previously withdrawn. Claims 1-10, 32-37 and 42 are currently pending, of which claims 1, 32 and 42 are independent. No new matter has been added.

### I. Summary of Claim Rejections

Claims 1-10 stand rejected under 35 U.S.C. §101.

Claims 1-10, 32-37 and 42 stand rejected under 35 U.S.C. §112, second paragraph.

Claims 1, 32 and 42 stand rejected under 35 U.S.C. §102(e) as being anticipated by United States Patent Number 7,167,817 to Mosterman et al. (hereafter "Mosterman").

Claims 1, 2, 6, 7, 10, 32, 36, 37 and 42 stand rejected under 35 U.S.C. §102(b) as being anticipated by United States Patent Number 6,411,923 to Stewart et al. (hereafter "Stewart").

Claims 1-7, 9-10, 32-37 and 42 stand rejected under 35 U.S.C. §102(b) as being anticipated by United States Patent Number 6,470,482 to Rostoker et al. (hereafter "Rostoker").

Claim 8 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Rostoker as applied to claim 2 in view of "SIMULINK Model-Based and System-Based Design," Version 4, by The MATHWORKS (hereafter "Simulink4").

### II. Claim Rejections under 35 USC §101

The Examiner rejected claims 1-10 under 35 U.S.C. §101 as allegedly being directed to non-statutory subject matter. More specifically, the Examiner asserted that "the claimed invention does not produce a useful, concrete, and tangible result. In particular, the invention is not limited to producing a tangible result" (Office Action, paragraph 2). Applicants respectfully traverse the 35 U.S.C. §101 rejection for at least the reasons set forth below.

Amended independent claim 1 recites "grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal in a graphical model *displayed on a graphical user interface.*" [emphasis added]

Applicants respectfully submit that amended claim 1 is directed to statutory subject matter for at least the following reasons. First, the bus signal is displayed for a user on a graphical user interface, and is thus a tangible result. Second, the result of the claimed invention is useful because the display of the bus signal provides the user information on the grouping of the first and second data signals in the graphical model. In view of the foregoing arguments, Applicants respectfully request reconsideration of the outstanding rejection of claim 1 under 35 U.S.C. §101.

Claims 2-10 depend from independent claim 1 and, as such, the above arguments apply to claims 2-10. Accordingly, Applicants also respectfully request reconsideration and allowance of claims 2-10.

**III. Claim Rejections under 35 USC §112**

The Examiner rejected claims 1-10, 32-37 and 42 under 35 U.S.C. §112, second paragraph, as allegedly being indefinite. More specifically, the Examiner asserted that independent claims recite "performing a non-virtual operation on the bus signal" which renders the claims vague and indefinite (Office Action, paragraph 3).

Applicants have amended the aforementioned claims to remove the phrase "non-virtual operation" that was discussed by the Examiner in the Office Action. Amended independent claims 1 and 32 now recite providing the bus signal as input to a non-virtual operation block. Similarly, amended independent claim 42 now recites performing an operation on a bus signal displayed in the graphical model. Accordingly, Applicants believe the amended claims to be in condition for allowance. Applicants respectfully request reconsideration of the outstanding rejection of claims 1, 32 and 42 under 35 U.S.C. §112, second paragraph.

Claims 2-10 depend from independent claim 1 and, as such, the foregoing amendments apply to claims 2-10. Accordingly, Applicants also respectfully request reconsideration and allowance of claims 2-10.

Claims 33-37 depend from independent claim 32 and, as such, the foregoing amendments apply to claims 33-37. Accordingly, Applicants also respectfully request reconsideration and allowance of claims 33-37.

## IV. Claim Rejections under 35 USC §102

### A. Claims 1, 32 and 42

The Examiner rejected claims 1, 32 and 42 under 35 U.S.C. §102(e) as being anticipated by Mosterman (Office Action, paragraph 4). Applicants respectfully traverse the 35 U.S.C. §102(e) rejections of claims 1, 32 and 42 for at least the reasons set forth below.

Mosterman discusses a method and apparatus of resolving artificial algebraic loops, that include providing an executable process having a plurality of functions (Mosterman, abstract). An analysis step identifies whether the process includes at least one potential artificial algebraic loop (Mosterman, abstract). If at least one potential artificial algebraic loop exists in the process, an artificial algebraic loop solution manipulates the order or manner by which the functions are executed to eliminate or otherwise resolve the artificial algebraic loop (Mosterman, abstract).

#### i) Claim 1

Amended independent claim 1 recites:

> "In an electronic device, a method comprising the steps of:
> grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal in a graphical model displayed on a graphical user interface;
> *providing the bus signal as input to a non-virtual operation block*; and
> performing an operation on the bus signal with the non-virtual operation block." [emphasis added]

Applicants respectfully submit that the Mosterman reference fails to disclose every feature of amended independent claim 1. Therefore, Mosterman does not support a valid 35 U.S.C. §102(e) rejection of claim 1. For example, Mosterman does not disclose at least the following feature of amended claim 1: "providing the bus signal as input to a non-virtual operation block."

The Examiner asserts in the Office Action at paragraph 4:

> "Regarding claims 1, 32, and 42, Mosterman discloses a system, medium, and method for generating and displaying a modeling application for simulating a dynamic system, comprising:
> ...an electronic device including memory for storing computer program instructions and data (FIG. 17, ref 315 and 316), and processor for executing the stored computer program instructions (FIG. 17, ref 311), the computer program instructions including instructions for performing a non-virtual operation on a bus signal displayed in the graphical model, wherein the bus signal comprises first data signal of a first signal type and a second data signal of a second signal type grouped to form the bus signal ["*A virtual block is provided for graphical organizational convenience and plays no role in the definition of the system of equations described by the block diagram model. Examples of virtual blocks are the Bus Creator virtual block and Bus Selector virtual block which are used to reduce block diagram clutter by managing groups of signals as a "bundle"*." (column 5, lines 10-27)."

The Examiner does not cite Mosterman as disclosing "providing the bus signal as input to a non-virtual operation block." Mosterman at column 5, lines 10-27, cited by the Examiner, discusses virtual blocks that manage groups of signals as a bundle. However, Mosterman does not disclose that the bundle of signals is provided as input to a non-virtual operation block, as required by claim 1. In fact, Applicants' Specification discusses the disclosure of grouping signals into a bundle in Mosterman as prior art (Specification, page 4, paragraph 1 and Figure 3). Applicants' Figure 3 illustrates such a virtual bus creator block and a bus selector block as discussed in Mosterman (Specification, page 12, last paragraph – page 13, first paragraph and Figure 3). In contrast, in the claimed invention as illustrated in Applicants' Figure 5, the bus signal *is provided as input to a non-virtual operation block.* Mosterman fails to disclose "providing the bus signal as input to a non-virtual operation block," as required by claim 1, in which the bus signal is a grouping of a first data signal of a first signal type and a second data

signal of a second signal type. In fact, Mosterman fails to address performing non-virtual operations on any type of bus signal or signal bundle.

For at least the reasons presented above, Applicants respectfully request reconsideration and allowance of claim 1.

ii) Claim 32

Amended independent claim 32 is a medium claim corresponding to amended independent claim 1 and recites:

> "In an electronic device, a medium holding computer-executable instructions for a method, comprising the steps of:
> grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal in a graphical model displayed on a graphical user interface;
> *providing the bus signal as input to a non-virtual operation block*; and
> performing an operation on the bus signal with the non-virtual operation block." [emphasis added]

Applicants submit that the arguments set forth above with respect to amended claim 1 are also applicable to amended claim 32. Accordingly, Applicants respectfully request reconsideration and allowance of claim 32.

iii) Claim 42

Amended independent claim 42 recites:

> "A system for generating and displaying a modeling application for simulating a dynamic system, comprising:
> user-operable input means for inputting data to the application;
> a display device for displaying a graphical model representing the dynamic system; and
> an electronic device including memory for storing computer program instructions and data, and a processor for executing the stored computer program instructions, the computer program instructions including instructions for *performing an operation on a bus signal displayed in the graphical model*, wherein the bus signal comprises a first data signal of a first signal type and a

> second data signal of a second signal type grouped together to form the bus signal." [emphasis added]

Applicants submit that the arguments set forth above with respect to amended claim 1 are also applicable to amended claim 42. Accordingly, Applicants respectfully request reconsideration and allowance of claim 42.

**B. Claims 1, 2, 6, 7, 10, 32, 36, 37 and 42**

The Examiner rejected claims 1, 2, 6, 7, 10, 32, 36, 37 and 42 under 35 U.S.C. §102(b) as being anticipated by Stewart (Office Action, paragraph 5). Applicants respectfully traverse the 35 U.S.C. §102(b) rejections of claims 1, 2, 6, 7, 10, 32, 36, 37 and 42 for at least the reasons set forth below.

Stewart discusses an analysis tool for aiding in the design of a process control system which conforms to a standard protocol (Stewart, abstract). The tool allows the efficient design of a process control system while ensuring that the physical characteristics of the system conform to the standard (Stewart, abstract).

**i) Claim 1**

Applicants respectfully submit that the Stewart reference fails to disclose every feature of amended independent claim 1. Therefore, Stewart does not support a valid 35 U.S.C. §102(b) rejection of claim 1. For example, Stewart does not disclose the following feature of amended claim 1: "providing the bus signal as input to a non-virtual operation block."

The Examiner asserts in the Office Action at paragraph 5:

> "Regarding claims 1, 2, 6, 7, 10, 32, 36, 37, and 42, Steward discloses a system, medium, and method for generating and displaying a modeling application for simulating a dynamic system, comprising:
> an electronic device including memory for storing computer program instructions and data (FIG. 1, ref 132); (column 4, lines 10-33), and a processor for executing the stored computer program instructions (FIG. 1, ref 134); (column 4, lines 10-33), the computer program instructions including instructions for performing a non-virtual operation on a bus signal displayed in the graphical

> model, wherein the bus signal comprises first data signal of a first signal type and a second data signal of a second signal type grouped to form a bus signal *["The Fieldbus protocol is an all digital, two-wire loop protocol." (column 2, lines 17-19); (FIG. 6A, 6B, etc.) showing bus segments connecting various "non-virtual" operational blocks, see (column 3, lines 28-42); (column 4, lines 10-33); (column 6, lines 40-67); etc.]*." [emphasis added]

The Examiner does not cite the Stewart reference as disclosing "providing the bus signal as input to a non-virtual operation block," as recited in claim 1. The Examiner asserts that the Figures 6A and 6B in Stewart show bus segments connecting various "non-virtual" operational blocks. Applicants respectfully disagree. Figures 6A and 6B in Stewart illustrate a bus structure composed of different configurable segments. The block-like structures running along the length of the bus structure are not labeled and are not disclosed to be non-virtual operation blocks. In addition, the Fieldbus bricks 612 in Figures 6A and 6B in Stewart are described as *junction portions* and are not *non-virtual operation blocks*. Stewart fails to disclose a non-virtual operation block, and therefore does not disclose providing a bus signal as input to a non-virtual operation block, as required by claim 1. As such, Applicants respectfully submit that Stewart fails to disclose the aforementioned feature of claim 1.

For at least the reasons presented above, Applicants respectfully request reconsideration and allowance of claim 1.

**ii) Claims 2, 6, 7 and 10**

Claims 2, 6, 7 and 10 depend from independent claim 1 and, as such, incorporate all of the elements of claim 1. Accordingly, claims 2, 6, 7 and 10 are allowable for at least the reasons set forth above with respect to claim 1. Applicants therefore respectfully request reconsideration and allowance of claims 2, 6, 7 and 10.

**iii) Claim 32**

Applicants submit that the arguments set forth above with respect to claim 1 are also applicable to claim 32. Accordingly, Applicants respectfully request reconsideration and allowance of claim 32.

iv) Claims 36 and 37

Claims 36 and 37 depend from independent claim 32 and, as such, incorporate all of the elements of claim 32. Accordingly, claims 36 and 37 are allowable for at least the reasons set forth above with respect to claim 32. Applicants therefore respectfully request reconsideration and allowance of claims 36 and 37.

v) Claim 42

Applicants submit that the arguments set forth above with respect to claim 1 are also applicable to claim 42. Accordingly, Applicants respectfully request reconsideration and allowance of claim 42.

C. Claims 1-7, 9-10, 32-37 and 42

The Examiner rejected claims 1-7, 9-10, 32-37 and 42 under 35 U.S.C. §102(b) as being anticipated by Rostoker (Office Action, paragraph 6). Applicants respectfully traverse the 35 U.S.C. §102(b) rejections of claims 1-7, 9-10, 32-37 and 42 for at least the reasons set forth below.

Rostoker discusses a system for interactive design, synthesis and simulation of an electronic system that allows a user to design a system either by specification of a behavioral model in a high level language such as VHDL or by graphical entry (Rostoker, abstract). The user can view full or partial simulation and design results simultaneously, on a single display window (Rostoker, abstract). The simulation results can be displayed immediately adjacent to signal lines on the diagram to which they correspond (Rostoker, abstract).

i) Claim 1

Applicants respectfully submit that the Rostoker reference fails to disclose every feature of amended independent claim 1. Therefore, Rostoker does not support a valid 35 U.S.C. §102(b) rejection of claim 1. For example, Rostoker does not disclose the following features of amended claim 1: (a) "grouping a first data signal of a first signal type and a second data signal

of a second signal type to form a bus signal in a graphical model displayed on a graphical user interface," (b) "providing the bus signal as input to a non-virtual operation block."

Applicants respectfully submit that Rostoker fails to disclose "grouping *a first data signal of a first signal type and a second data signal of a second signal type* to form a bus signal in a graphical model displayed on a graphical user interface," as recited in claim 1.

The Examiner asserts in the Office Action at paragraph 6:

> "Regarding claim 1, Rostoker discloses a method comprising the steps of:
> Grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal in a graphical model displayed on a graphical user interface ["*A bus signal line 2220 (CTRL<0...3>, representing four physical "wires") connects between the graphical representation 2216 of the microprocessor 2116 and the graphical representation 2214 of the controller 2114 and extends off towards the right hand side of the display screen 2200 (as depicted).*" (column 32, lines 46-51)]; and
> Performing a non-virtual operation on the bus signal [the bus 2220 connects to graphical representation 2214 of the controller 2114, and "The design description 2114a for the other 2114 (CHIP 3) refers to a core cell 2128 (CORE 'C') and a logic block 2130 (misc. logic 'C')." (column 32, lines 31-33)."

It appears from the Office Action that the Examiner is pointing to the bus signal line 2220 in the Rostoker reference as disclosing the bus signal as recited in Applicants' claim 1. Applicants respectfully disagree. The cited sections of Rostoker fail to disclose "*grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal* in a graphical model, the bus signal displayed on a graphical user interface," as required by claim 1. Rostoker at column 32, lines 46-51, cited by the Examiner, discusses a bus signal line as four virtual wires connecting the graphical representation of a microprocessor with the graphical representation of a controller. Furthermore, Rostoker at column 32, lines 53-55 simply states that the bus signal line carries *simulation results*. In contrast, claim 1 requires that the bus signal is a grouping of a first data signal of *a first signal type* and a second data signal of *a second signal type*. Rostoker does not address the signal types of the simulation results carried by the bus signal line 2220, and specifically fails to disclose that the bus signal line 2220 is a grouping of a first data signal of a first signal type and a second data signal of a second signal type, as required by claim 1.

Applicants respectfully submit that Rostoker also fails to disclose "providing the bus signal as input to a non-virtual operation block," as required by claim 1. The Examiner points to the misc. logic block 2130 in the chip 3 design description in Figure 21b as performing a non-virtual operation. Applicants respectfully disagree since Rostoker does not disclose that the logic block 2130 of the controller performs a non-virtual operation on the bus signal line. As such, Applicants respectfully submit that Rostoker fails to disclose the above feature of claim 1.

For at least the reasons presented above, Applicants respectfully request reconsideration and allowance of claim 1.

**ii) Claims 2-7 and 9-10**

Claims 2-7 and 9-10 depend from independent claim 1 and, as such, incorporate all of the elements of claim 1. Accordingly, claims 2-7 and 9-10 are allowable for at least the reasons set forth above with respect to claim 1. Applicants therefore respectfully request reconsideration and allowance of claims 2-7 and 9-10.

**iii) Claim 32**

Applicants submit that the arguments set forth above with respect to claim 1 are also applicable to claim 32. Accordingly, Applicants respectfully request reconsideration and allowance of claim 32.

**iv) Claims 33-37**

Claims 33-37 depend from independent claim 32 and, as such, incorporate all of the elements of claim 32. Accordingly, claims 33-37 are allowable for at least the reasons set forth above with respect to claim 32. Applicants therefore respectfully request reconsideration and allowance of claims 33-37.

v) Claim 42

Applicants submit that the arguments set forth above with respect to claim 1 are also applicable to claim 42. Accordingly, Applicants respectfully request reconsideration and allowance of claim 42.

## V. Claim Rejections under 35 USC §103

The Examiner rejected claim 8 under 35 U.S.C. §103(a) as being unpatentable over Rostoker as applied to claim 2 in view of the Simulink4 reference (Office Action, paragraph 7). Applicants respectfully traverse the 35 U.S.C. §103(a) rejection of claim 8 for at least the reasons set forth below.

Claim 8 depends from independent claim 1. Applicants respectfully submit that Rostoker and Simulink4, alone or in any reasonable combination, fail to disclose or suggest all of the features of claim 8.

Applicants respectfully submit that Rostoker and Simulink4 fail to disclose or suggest at least the following features of claim 8: (a) "*grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal* in a graphical model displayed on a graphical user interface," and (b) "performing an operation on the bus signal with the *non-virtual operation block*."

Rostoker has been summarized above. As discussed previously, Rostoker fails to disclose or suggest the aforementioned features of claim 8. The teachings of Simulink4 do not supplement Rostoker in such a way as to cure Rostoker's failure to disclose or suggest the above features of claim 8.

Simulink4 provides general instructions on the use of SIMULINK for performing model-based and system-based design, and fails to disclose or suggest "grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal in a graphical model displayed on a graphical user interface," or "performing an operation on the bus signal with the non-virtual operation block." Therefore, Rostoker and Simulink4, alone or in

any reasonable combination, do not support a valid 35 U.S.C. §103(a) rejection of claim 8. Accordingly, Applicants respectfully request reconsideration and allowance of claim 8.

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## CONCLUSION

In view of the foregoing claim amendments and remarks, Applicants believe that all claims should be passed to issuance.

Please charge any shortage or credit any overpayment of fees to our Deposit Account No. 12-0080, under Order No. MWS-058. In the event that a petition for an extension of time is required to be submitted herewith, and the requisite petition does not accompany this response, the undersigned hereby petitions under 37 C.F.R. §1.136(a) for an extension of time for as many months as are required to render this submission timely. Any fee due is authorized to be charged to the aforementioned Deposit Account.

Should the Examiner feel that a teleconference would expedite the prosecution of this application, the Examiner is urged to contact the Applicants' attorney at (617) 227-7400.

Dated: May 16, 2007

Respectfully submitted,

By /John S. Curran/
John S. Curran
Registration No.: 50,445
LAHIVE & COCKFIELD, LLP
One Post Office Square
Boston, Massachusetts 02109-2127
(617) 227-7400
(617) 742-4214 (Fax)
Attorney/Agent For Applicant